

SPECIFICATION

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MULTI-PORT MEMORY CELLS

Cross Reference to Related Applications

This is a continuation-in-part of patent applications, titled: "Dual-Port Memory Cell", now U.S. Pat. No. 6,552,951, USSN 09/806,299 (Attorney docket number: 98P-02816W0US) and "Memory Architecture with Refresh and Sense Amplifiers", USSN 10/131,364 (Attorney docket number: 00P-19334U501).

Background of Invention

[0001] Integrated circuits (ICs) can include an array of dynamic random access memory cells. Each memory cell comprises a storage node carrying a charge which represents the information to be stored. The charge stored within the storage node leaks due to parasitic current paths. The storage node has to be refreshed prior to the charge leaking beyond a threshold value which can be detected by a sense amplifier. During a refresh cycle, information stored in the memory cells are read out, amplified, and written back into the memory cells.

[0002] When the memory cells are refreshed, access to the array is prevented. This is because the refresh operation must be prioritized over a memory access to ensure that the information stored in the memory cells is maintained. As such, when both access and refresh are requested, the access is delayed until the refresh is completed. Thus, performance is adversely impacted by refresh operation.

[0003] From the foregoing discussion, it is desirable to provide a memory array which reduces the adverse impact of the refresh operation.

Summary of Invention

[0004] The invention relates to ICs with a memory array. More particularly, the invention relates to improving performance of the memory array. In one embodiment, a memory